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HP References in this Manual

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HP E2419A

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	Yes	No
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2. Were you satisfied with the operation of the product at turn-on?	[ ]	[ ]

3. Were the proper accessories supplied with your product?

If not, what was missing?

Cables [ ] Manual(s) [ ] Other _____

4. What measurements will this product be used to make?_____

_____.

5. Which logic analyzer are you using?

Type_____

6. What do you like most about the product? _____

_____

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[ ] Installation Overview
[ ] Step-By-Step Procedures
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10. What is your experience with logic analyzers?

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[ ] Less than 1 year experience
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HP 1650A/B and HP 1651A/B

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HP E2419A Motorola MC68HC16 EVB Logic Analysis Support and MC68HC16 Preprocessor Interface User's Guide

for the HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A Logic Analyzers

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List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in the Printing History and on the title page.

Pages	**Effective Date**

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This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this user's guide must be heeded.

Contents

Chapter 3: General Information

Appendix A: Troubleshooting

Introduction

This user's guide includes information on using the HP E2419A Preprocessor Interface to do logic analysis on the MC68HC16 microprocessor or Motorola MC68HC16 Evaluation Board (EVB). The HP E2419A Preprocessor Interface provides a complete interface between any Motorola MC68HC16 target system or MC68HC16 EVB and the following logic analyzers: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, or HP 16550A.

Since there is no active circuitry between the microprocessor and the logic analyzer to add skew to signals, the preprocessor interface can be used for timing analysis as well as state analysis.

The HP E2419A configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the MC68HC16 microprocessor and the MC68HC16 EVB. It also loads the inverse assembler for obtaining displays of microprocessor data in the assembly language mnemonics of the microprocessor.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2419A Preprocessor Interface:

HP 1650A, HP 1650B, HP 1652B, HP 16510A, and HP 16510B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 1650A or HP 16510A) or 80 channels of 100 MHz timing analysis.

HP 1660A/61A/62A

The HP 1660A/61A/62A Logic Analyzers provide 4 k of memory depth with 136 channels (HP 1660A), 102 channels (HP 1661A), or 68 channels (HP 1662A) of 100 MHz state analysis or 250 MHz timing analysis. These logic analyzers also support various combinations of mixed state/timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis, or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing analysis.

HP 16540A,D with one or two HP 16541A,D Expansion Cards

This logic analyzer combination provides 4 k of memory depth (16 k with the D version) with either 64 or 112 channels of 100 MHz state or timing analysis.

HP 16542A (Master Card and two or three expansion cards)

This logic analyzer combination provides 1 M of memory depth with 48 or 64 channels of 100 MHz state or timing analysis.

HP 16550A

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz timing analysis. The logic analyzer will also support various combinations of mixed state/timing analysis.

How to Use This Manual

This manual is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP E2419A Preprocessor Interface to perform measurements with the supported logic analyzers.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP E2419A software. It also provides information about the inverse assembler and status encoding.
- Chapter 3 contains additional reference information including the characteristics and signal mapping for the HP E2419A Preprocessor Interface. It also contains information on servicing.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

1

Setting Up the HP E2419A

Introduction

This chapter explains how to install and configure the HP E2419A Preprocessor Interface to perform MC68HC16 or MC68HC16 EVB measurements with the supported logic analyzers.

Duplicating the Master Disk

Before you use the HP E2419A software, use the Duplicate Disk operation in the disk menu of your logic analyzer to make a duplicate copy of the HP E2419A master disk. Then store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidently deleted.

Equipment Supplied

The HP E2419A Preprocessor Interface consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor interface circuit card.
- The configuration files and inverse assembler software on a 3.5-inch disk.
- The QFP Probe Adapter Assembly, which includes the *QFP Probe Adapter Assembly Operating Note*.
- This user's guide.

Note 

The preprocessor interface socket assembly pins are covered at the time of shipment with a protective foam pad. This is done to protect the delicate gold plated pins of the assembly from damage due to impact. When you're not using the preprocessor interface, protect the socket assembly pins from damage by covering them with the foam protector.

Equipment Required

The minimum equipment required for state analysis of MC68HC16 target systems or the MC68HC16 EVB consists of the following items:

- An HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, or HP 16550A Logic Analyzer.
- The HP E2419A Preprocessor Interface, including the QFP Probe Adapter Assembly.
- Three to six 100 kOhm Termination Adapters (HP part number 01650-63203) for analysis of MC68HC16 EVB systems. The termination adapters are not shipped with the preprocessor interface. As an alternative, you can use the General Purpose Probes shipped with your logic analyzer to analyze MC68HC16 EVB systems.

Note 

The above equipment is the minimum required for three-pod state analysis. There are three additional pods on the preprocessor interface which can be monitored; however, the three optional pods require either the General Purpose Probes shipped with your logic analyzer, or one 100 kOhm Termination Adapter per pod (HP part number 01650-63203).

Installation Overview

The following procedures describe the major steps required to install the hardware and software for MC68HC16 or MC68HC16 EVB measurements. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

Caution 

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface or logic analyzer is being connected or disconnected.

MC68HC16 Microprocessors

1. Install the QFP Probe Adapter Assembly on the target system microprocessor (see the *QFP Probe Adapter Assembly Operating Note*).
2. Connect the preprocessor interface to the QFP Probe Adapter Assembly (see page 1-5).
3. Plug the logic analyzer pods into the preprocessor interface (see page 1-6).
4. Load the logic analyzer configuration and inverse assembler by loading the appropriate file from the disk (see page 1-14).

MC68HC16 EVB

1. Connect the 100 kOhm Termination Adapters (HP part number 01650-63203) to the MC68HC16 EVB (see page 1-11).
2. Plug the logic analyzer cables into the termination adapters on the MC68HC16 EVB (see page 1-11).
3. Load the logic analyzer configuration file and inverse assembler for the logic analyzer you are using (see page 1-14).

You are now ready to make measurements with the logic analyzer. The rest of this chapter contains more detailed information on setting up the hardware and software.

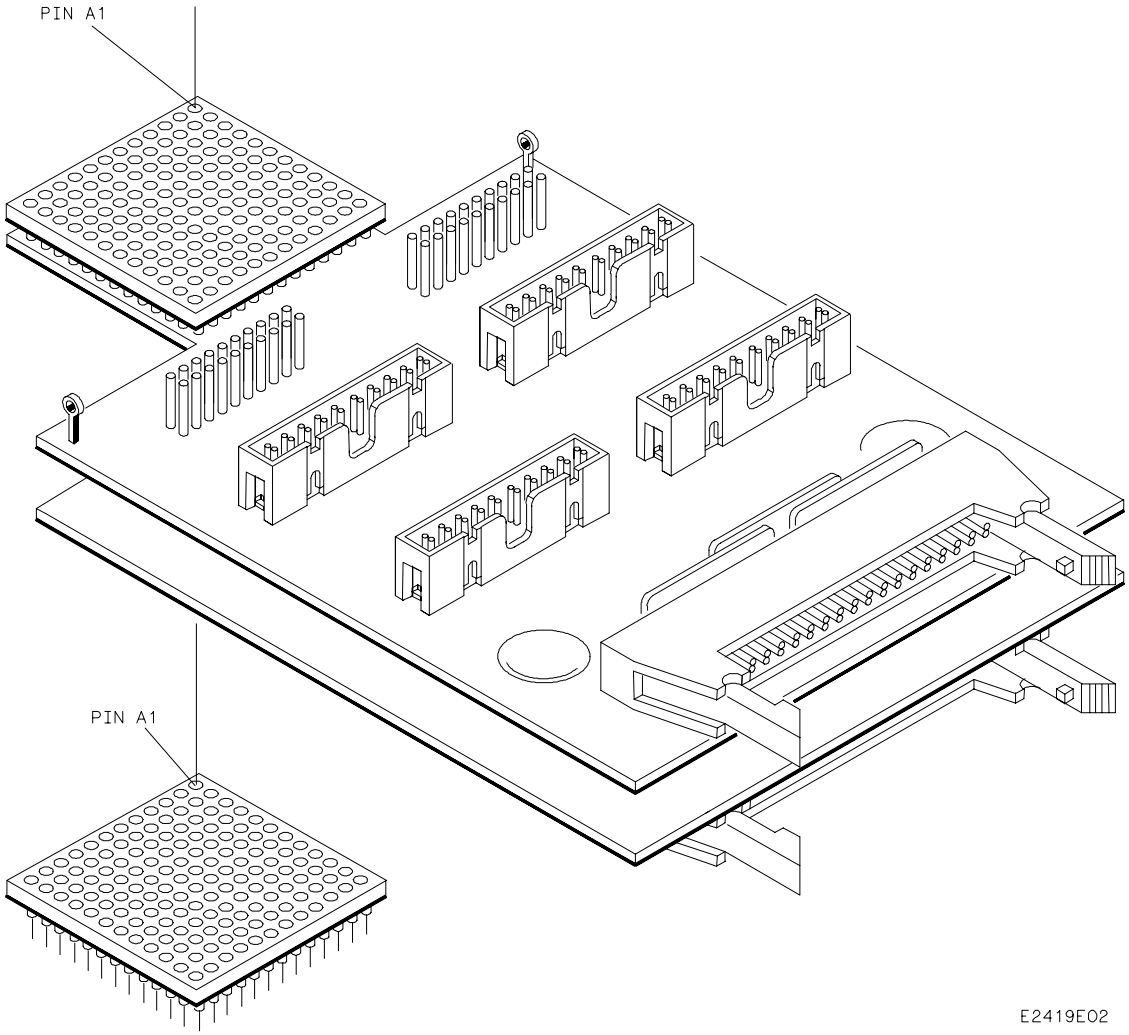

Figure 1-1. HP E2419A Preprocessor Interface

Connecting to the MC68HC16

The HP E2419A Preprocessor Interface requires a QFP Probe Adapter Assembly for connecting to the MC68HC16 microprocessor. The probe adapter assembly allows the preprocessor interface to be connected without removing the microprocessor from the target system. The following steps explain how to connect the HP E2419A Preprocessor Interface to your target system:

Caution 

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface or probe adapter assembly is being connected or disconnected.

1. Using the instructions in the *QFP Probe Adapter Assembly Operating Note*, connect the probe adapter assembly to the target system microprocessor. Ensure that pin 1 is properly aligned.

Caution 

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin 1 and pin A1 on the preprocessor interface, probe adapter assembly, and microprocessor prior to making any connection. Also, take care to align the preprocessor interface connector with the pins on the probe adapter assembly so that all pins are making contact.

2. Install the preprocessor interface probe into the PGA socket on the adapter probe, again ensuring that pin A1 is properly aligned.

Connecting to the HP E2419A

Connect the logic analyzer cables to the preprocessor interface as shown in table 1-1. Note that if you are connecting to an MC68HC16 EVB, without using the preprocessor interface, you must use the connections in table 1-2 (see page 1-12). Descriptions such as P1 refer to connectors on the preprocessor interface, while Pod 1 refers to a logic analyzer pod. Preprocessor interface connectors P1, P3, and P5 are required for inverse assembly, while P2, P4, and P6 are optional. P1, P3, and P5 can be connected directly to the logic analyzer, while P2, P4, and P6 require termination adapters or General Purpose Probes (see "Connecting the Termination Adapters to the Preprocessor Interface").

Figure 1-2 shows the relative locations of the logic analyzer cards.

Note

HP 16542A with three or four Expansion Cards

The locations for the HP 16542A expansion cards, relative to the Master Card, depend on the number of expansion cards used. If one or two expansion cards are used, Card 1 is located above the Master Card and Card 2 is located below the Master Card. If three expansion cards are used, two of them are located above the Master Card and the third is located below the Master Card. When four expansion cards are used, they are located as shown in figure 1-2.

Tables 1-1 and 1-2 show the physical location and connections for a two-expansion-card and a three-expansion-card system. If you are using more expansion cards, and want to connect additional pods, check the Format menu in the logic analyzer to see where the pods should be connected.

Power Up / Down Sequence

When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, and then the logic analyzer.

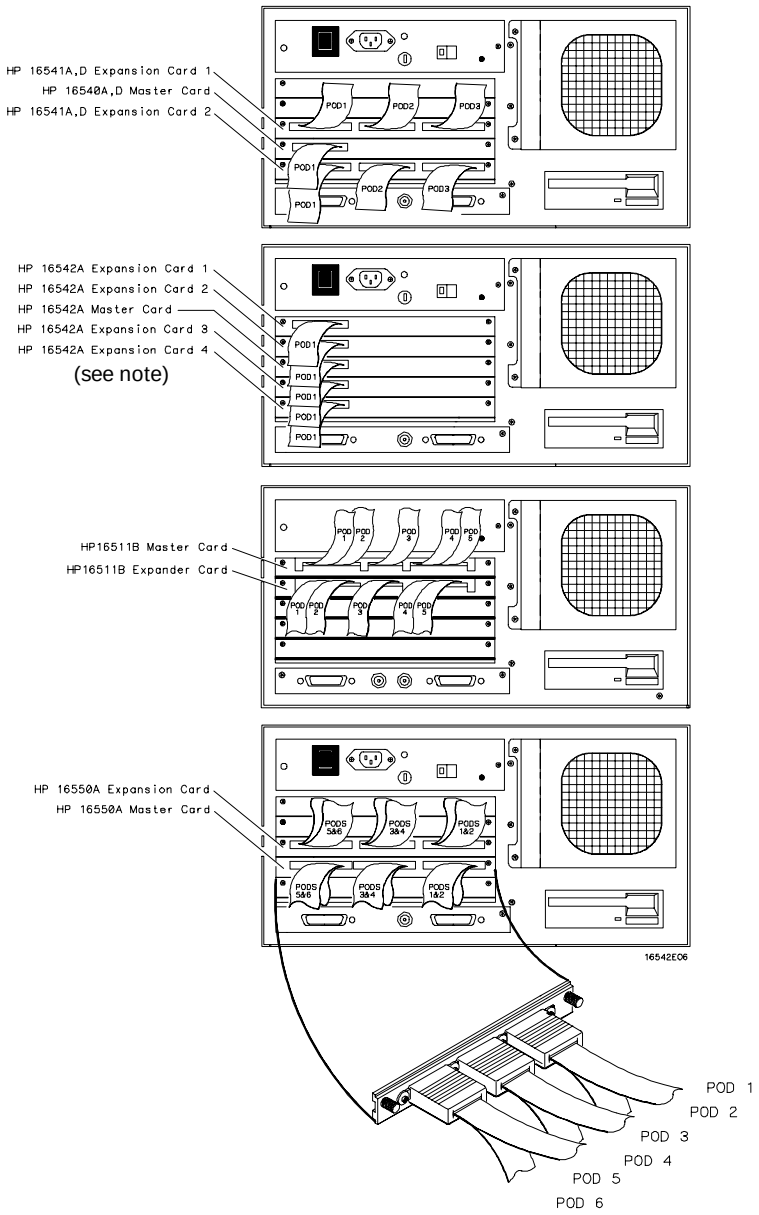

Figure 1-2. Logic Analyzer Card Locations
(relative locations, actual slots used may vary)

Table 1-1. HP E2419A Connections and Configuration Files for MC68HC16 Analysis (HP 1650 series, HP 16510A/B, HP 16511B, HP 16540/16541A,D, HP 16550A)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A, HP 1650B, HP 16510A, HP 1652B and HP 16510B	CHC16		P5 STAT	P4 ADDR (1, 2)	P3 ADDR	(1, 2, 3)	P1 DATA clk ↑
HP 16511B Upper Card	DHC16		--	--	--	--	--
HP 16511B Lower Card			P5 STAT	P4 ADDR (1, 2)	P3 ADDR	(1, 2, 3)	P1 DATA clk ↑
HP 16541A,D Exp. Card 1 (4)	EHC16		--	--	P5 STAT	P4 ADDR (1, 2)	P3 ADDR
HP 16540A,D Master Card			--	--	--	--	P1 DATA clk ↑
HP 16541A,D Exp. Card 1 (4)	EHC16_6				P5 STAT	P4 ADDR (1, 2)	P3 ADDR
HP 16540A,D Master Card							P1 DATA clk ↑
HP 16541A,D Exp. Card 2 (4)					--	P6 (1, 2)	P2 (1, 2)
HP 16550A	FHC16	P6 (1, 2)	P5 STAT	P4 ADDR (1, 2)	P3 ADDR	P2 (1, 2)	P1 DATA clk ↑

1 This logic analyzer pod does not have to be connected to a preprocessor interface connector for inverse assembly.
2 Use of this logic analyzer pod requires a termination adapter (see "Connecting the Termination Adapters").
3 As an option, you can connect this logic analyzer pod to P2 or P6.
4 For the HP 16541A,D Expander Cards, Exp. Card 1 refers to the physically highest HP16541A,D card, and Exp. Card 2 refers to the next physically highest HP 16541A,D card (see figure 1-2).

Table 1-1. HP E2419A Connections and Configuration Files for MC68HC16 Analysis (HP 1660 series, HP 16542A)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 16542A Exp. Card 1 (3)	EHC16						P5 STAT
HP 16542A Master Card							P1 DATA clk↑
HP 16542A Exp. Card 2 (3)							P3 ADDR
HP 16542A Exp. Card 1 (3)	EHC16						P5 STAT
HP 16542A Exp. Card 2 (3)							P4 ADDR (1, 2)
HP 16542A Master Card							P1 DATA clk↑
HP 16542A Exp. Card 3 (3)							P3 ADDR
HP 1662A	FHC16			P4 ADDR (1, 2)	P3 ADDR	P5 STAT	P1 DATA clk↑
HP 1661A	FHC16	P6 (1, 2)	P5 STAT	P4 ADDR (1, 2)	P3 ADDR	P2 (1, 2)	P1 DATA clk↑
HP 1660A	FHC16	**(Pod 8)** P6 (1, 2)	**(Pod 7)** P5 STAT	P4 ADDR (1, 2)	P3 ADDR	P2 (1, 2)	P1 DATA clk↑

1 This logic analyzer pod does not have to be connected to a preprocessor interface connector for inverse assembly.
2 Use of this logic analyzer pod requires a termination adapter (see "Connecting the Termination Adapters").
3 For the HP 16542A Expander Cards, Exp. Card 1 refers to the physically highest HP16542A Expansion Card, and Exp. Card 2 refers to the next physically highest HP 16542A Expansion Card (see figure 1-2).

Connecting the Termination Adapters to the Preprocessor Interface

The logic analyzer probes must be properly terminated for the logic analyzer to operate correctly. On the preprocessor interface, there are nine connectors. P1, P3, and P5 have both terminated and nonterminated connectors, while P2, P4, and P6 only have nonterminated connectors. The terminated connectors (wide 2 x 20 connectors) for P1, P3, and P5 can be connected directly to the logic analyzer. You can probe P2, P4, and P6 with the General Purpose Probes shipped with your logic analyzer, or use 100 kOhm Termination Adapters (HP part number 01650-63203). The following steps explain how to connect the termination adapters to the preprocessor interface:

1. Align the key on the male end of the termination adapter with the slot on the connector of one of the logic analyzer cables, and push the termination adapter into the connector.
2. Connect the female end of the termination adapter to the preprocessor interface.
3. Repeat steps 1 and 2 for each termination adapter.

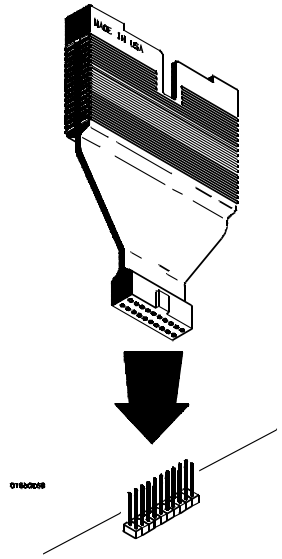

Figure 1-3. Connecting the Termination Adapter

Connecting to the MC68HC16 EVB

The MC68HC16 EVB evaluation board contains seven 2 x 10 nonterminated connectors, labelled P1 through P7. These connectors can be probed with either the General Purpose Probes shipped with your logic analyzer, or by using three to six 100 kOhm Termination Adapters (HP part number 01650-63203). The termination adapters are not shipped with the HP E2419A Preprocessor Interface. The configuration software sets up the logic analyzer for MC68HC16 EVB analysis.

Only three connectors are required for inverse assembly; P1, P2, and P5. Connectors P3, P4, and P6 are optional.

Note 

The connectors on the MC68HC16 EVB are numbered differently than the connectors on the preprocessor interface hardware. The signal-to-connector tables in Chapter 3 list the signals according to the preprocessor interface pod numbers.

To connect the MC68HC16 EVB to the logic analyzer using the termination adapters, use the following procedures:

1. With the key on the termination adapter facing the center of the MC68HC16 EVB board, align the termination adapter with the appropriate connector on the MC68HC16 EVB (see table 1-2 to determine which MC68HC16 EVB connectors to use).
2. Push the termination adapter into the connector.
3. Repeat steps 1 and 2 for each termination adapter.
4. Plug the logic analyzer cables into the termination adapters on the MC68HC16 EVB as listed in table 1-2. Descriptions such as P1 refer to connectors on the MC68HC16 EVB, while Pod 1 refers to a logic analyzer pod. Figure 1-2 shows the relative locations of the logic analyzer cards. For the HP 16542A Logic Analyzer, see note on page 1-6.

Table 1-2. Connections and Configuration Files for MC68HC16 EVB Analysis (HP 1650 series, HP 16510A/B, HP 16511B, HP 16540/16541A,D, HP 16550A)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A, HP 1650B, HP 16510A, HP 1652B and HP 16510B	CHC16		P5 STAT	P3 ADDR (1)	P1 ADDR	(1, 2)	P2 DATA clk ↑
HP 16511B Upper Card	DHC16						
HP 16511B Lower Card			P5 STAT	P3 ADDR (1)	P1 ADDR	(1, 2)	P2 DATA clk ↑
HP 16541A,D Exp. Card 1 (3)	EHC16		--	--	P5 STAT	P3 ADDR (1)	P1 ADDR
HP 16540A,D Master Card			--	--	--	--	P2 DATA clk ↑
HP 16541A,D Exp. Card 1 (3)	EHC16_6		--	--	P5 STAT	P3 ADDR (1)	P1 ADDR
HP 16540A,D Master Card			--	--	--	--	P2 DATA clk ↑
HP 16541A,D Exp. Card 2 (3)			--	--		P6 (1)	P4 (1)
HP 16550A	FHC16	P6 (1)	P5 STAT	P3 ADDR (1)	P1 ADDR	P4 (1)	P2 DATA clk ↑

1 This logic analyzer pod does not have to be connected to an MC68HC16 EVB connector for inverse assembly.
2 As an option, you can connect this logic analyzer pod to P4 or P6.
3 For the HP 16541A,D Expander Cards, Exp. Card 1 refers to the physically highest HP16541A,D card, and Exp. Card 2 refers to the next physically highest HP 16541A,D card (see figure 1-2 on page 1-7).

Table 1-2. Connections and Configuration Files for MC68HC16 EVB Analysis (HP 1660 series, HP 16542A)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 16542A Exp. Card 1 (2)	EHC16						P5 STAT
HP 16542A Master Card							P2 DATA clk↑
HP 16542A Exp. Card 2 (2)							P1 ADDR
HP 16542A Exp. Card 1 (2)	EHC16						P5 STAT
HP 16542A Exp. Card 2 (2)							P3 ADDR (1)
HP 16542A Master Card							P2 DATA clk↑
HP 16542A Exp. Card 3 (2)							P1 ADDR
HP 1662A	FHC16			P3 ADDR (1)	P1 ADDR	P5 STAT	P2 DATA clk↑
HP 1661A	FHC16	P6 (1)	P5 STAT	P3 ADDR (1)	P1 ADDR	P4 (1)	P2 DATA clk↑
HP 1660A	FHC16	**(Pod 8)** P6 (1)	**(Pod 7)** P5 STAT	P3 ADDR (1)	P1 ADDR	P4 (1)	P2 DATA clk↑

1 This logic analyzer pod does not have to be connected to an MC68HC16 EVB connector for inverse assembly.
2 For the HP 16542A Expander Cards, Exp. Card 1 refers to the physically highest HP16542A Expansion Card, and Exp. Card 2 refers to the next physically highest HP 16542A Expansion Card (see figure 1-2 on page 1-7).

Setting Up the Analyzer from the Disk

The logic analyzer is configured for state analysis by loading the appropriate configuration file. Loading this file also loads the inverse assembler. To load the configuration and inverse assembler:

1. Install the HP E2419A disk in the front disk drive of the logic analyzer.
2. Select one of the following menus:
   - For the HP 1650-series logic analyzers, select the I/O Disk Operations menu;
   - For the HP 16500-series and HP 1660-series logic analyzers, select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer configuration from disk.
4. For HP 16500-series and HP 1660-series logic analyzers, select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.
5. Use the knob to select the appropriate configuration file (see table 1-1 or 1-2).
6. Execute the load operation to load the file into the logic analyzer.

Timing Analysis

The format specification loaded for state analysis may also be used for timing analysis. To configure the logic analyzer for timing analysis:

1. Load the appropriate state configuration file from the disk.
2. Select the Configuration menu of the logic analyzer.
3. Select the Type field and select Timing.

Probing With an Oscilloscope

The individual pins on the preprocessor interface can also be probed with an oscilloscope. There are two ground pins on the top of the preprocessor interface (see figure 1-4). Connect the ground lead of the oscilloscope probe to one of the ground pins on the preprocessor interface, and the other lead to the signal to be measured. The signals which are on the preprocessor interface are listed in table 3-2.

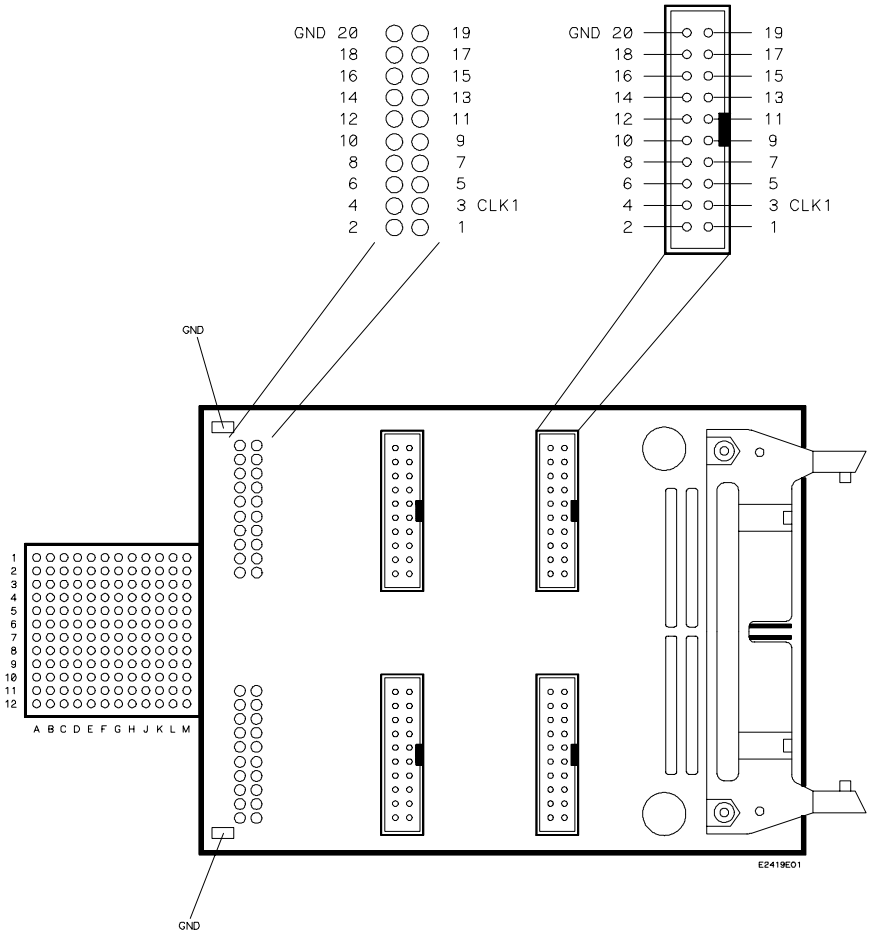

Figure 1-4. Pin Numbers and Ground Pins

2

Analyzing the MC68HC16 or MC68HC16 EVB

Introduction

This chapter provides reference information on the format specifications and symbols configured by the HP E2419A software. It also provides information about the inverse assembler and status encoding.

Format Specification

The format specification for the logic analyzer is set up by the HP E2419A software similar to that shown in figures 2-1 and 2-2. There will be some slight differences in the displays, according to which logic analyzer you are using. For example, some logic analyzers do not have a Clock Period field. Refer to your logic analyzer manual to see which fields and displays are available.

The label DATA_B is included in the format specification to give you a convenient method of displaying the microprocessor data in both hexadecimal and mnemonic formats. This field makes it easier to specify a trace specification from the data in the listing menu.

Chapter 3 lists the microprocessor signals for the HP E2419A and their corresponding lines to the logic analyzer.

Note

For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B), the Clock Period field in figures 2-1 and 2-2 should remain in the current selection (> 60 ns) for proper HP E2419A operation. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

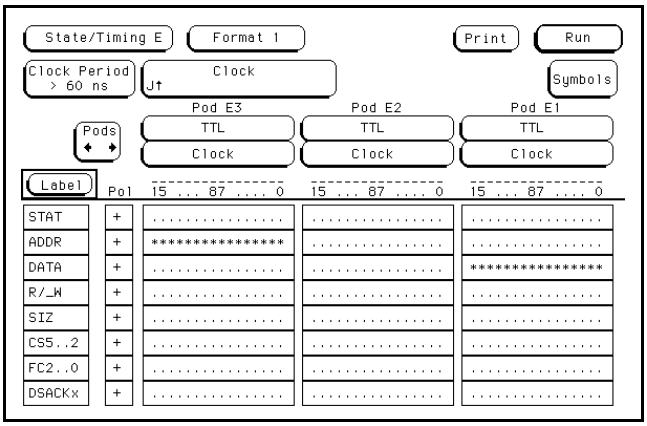

Figure 2-1. Format Specification (Pods 1 - 3)

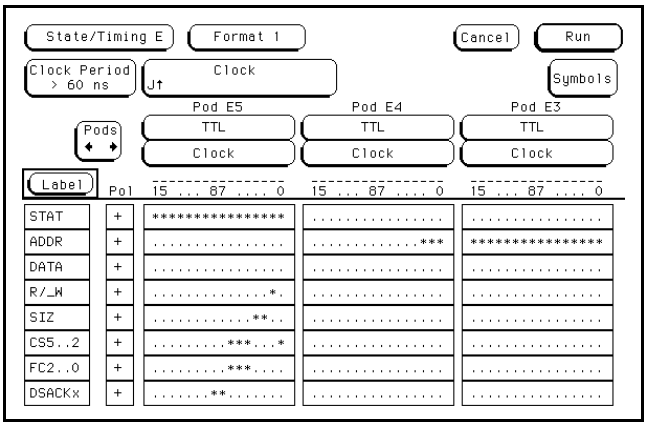

Figure 2-2. Format Specification (Pods 3 - 5)

Symbols

The configuration files set up symbol tables on the logic analyzer. The tables contain alphanumeric values which identify data patterns or ranges. Table 2-1 lists a description of the bits in the STAT label. Table 2-2 lists the Status Field Encoding. Table 2-3 lists some additional symbols.

Table 2-1. STAT Label Bits

Bit	Status Signals	Description
0	BGACK/CS2	This signal is low when the microprocessor has granted control of the bus to another device. *
1	R/W	This signal is high for read cycles and low for write cycles.
2-3	SIZ0-SIZ1	These signals indicate the size of the bus transfer from the microprocessor.
4-6	FC0-FC2	These signals indicate the type of cycle the microprocessor is executing. *
7-8	DSACK0-DSACK1	These signals indicate the size of the bus transfer to the microprocessor that was completed.
9	IPIPE1 Phase2	These signals indicate instruction pipeline activity.
10	IPIPE0 Phase2	
11	IPIPE1 Phase1	
12	IPIPE0 Phase1	
13	FREEZE	This signal indicates the CPU is in background mode.
14	BKPT/DSCLK	This signal indicates a hardware breakpoint to the CPU.
15	BERR	This signal indicates a bus error.

* These signals may alternately be configured as chip selects.

Table 2-2. Status Field Encoding

	Status Bit			
Microprocessor Cycle Type	**15 14 13 12**	**11 10 9 8**	**7 6 5 4**	**3 2 1 0**
Fetch	x x x x	0 x x x	x x x x	x x 1 x
Data Read	x x x x	1 x x x	x x x x	x x 1 x
Data Write	x x x x	1 x x x	x x x x	x x 0 x
Read	x x x x	x x x x	x x x x	x x 1 x
Write	x x x x	x x x x	x x x x	x x 0 x
Data	x x x x	1 x x x	x x x x	x x x x
Bus Error	0 x x x	x x x x	x x x x	x x x x
Size of Transfer				
Byte Transfer	x x x x	x x x x	x x x x	0 1 x x
Word Transfer	x x x x	x x x x	x x x x	1 0 x x
3-Byte Transfer	x x x x	x x x x	x x x x	1 1 x x
Long Word Transfer	x x x x	x x x x	x x x x	0 0 x x
IPIPE Encoding	**12 11 10 9**			
Invalid	x x 0 0			
Exception	x x 0 1			
Advance	x x 1 0			
Null (not an instruction)	1 1 1 1			
Start (prefetched instruction is executing)	0 x x x			
Fetch (this is part of an instruction fetch)	x 0 x x			
Start and Fetch	0 0 x x			

Table 2-3. HP E2419A Symbols

Label	Symbol	Pattern
SIZ	byte word 3 byte long	0 1 1 0 1 1 0 0
R/_W	write read	0 1
DSACK	wait 8 bit 16bit rsvd	1 1 1 0 0 1 0 0

Listing Menu

Captured data is displayed as shown in figure 2-3. This figure displays the state listing for 16-bit bus cycles. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

The logic analyzer always probes the full 16-bit data bus of the microprocessor. There are some instructions that use only 8 bits for memory transactions. When fewer than the full 16 bits of the data bus are used by a memory cycle, the inverse assembler marks the bits not used by the microprocessor with an "x."

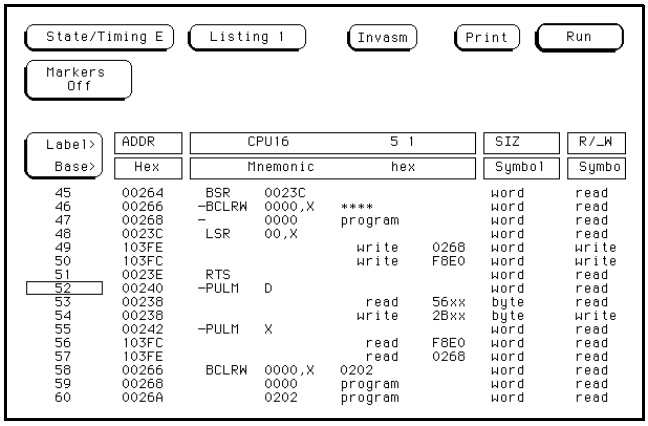

Figure 2-3. State Listing

The Inverse Assembler

The microprocessor does not provide enough status information for the inverse assembler to pick out the first word of an opcode fetch from a series of program reads. For correct disassembly, you must point to the 16-bit word that contains the first word of an opcode fetch. Once synchronized, the inverse assembler disassembles from this point through the last line of the display. To point to the first word of an opcode fetch:

1. Select a line on the display that you know contains the first word of an instruction fetch.
2. Roll this line to the top of the display.

Note 

The cursor location is not the top of the display. In figure 2-3, line 45 is the top of the display.

---

3. Select the "Invasm" field at the top of the display. The listing inverse assembles from the top line down. Any data before this display is left unchanged.

Rolling the display up inverse assembles the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you may have to re-synchronize the inverse assembler by repeating steps 1 through 3.

Note 

Each time you inverse assemble a block of memory, the analyzer keeps that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Interpreting Data

In general, asterisks indicate that expected operand fetches are not stored in the logic analyzer memory. Four asterisks (****) indicate that one word of an expected operand was missing. Missing operands (or parts of operands) can result from microprocessor instruction prefetch activity or storage qualification.

Example:

```
BCLRW    0000,X          ****
```

The microprocessor is capable of supporting byte and word operands. During operand reads and writes, entire 16-bit (word) values appear on the microprocessor data bus. In the case of single-byte operands, the inverse assembler displays "xx" for the byte of the input data that is ignored by the microprocessor. In this manner, you can determine exactly which byte of data the microprocessor has used as an operand.

Unused Prefetches (–/?)

The microprocessor may fetch up to two instruction words while the last opcode is still being executed. When a program executes an instruction that causes a branch, prefetched words are not used and are discarded by the microprocessor. Unused prefetches are indicated by the prefix "–" in the inverse assembly listing, as shown in lines 46, 47, 52, and 55 of figure 2-3 on page 2-6.

In some cases, it is impossible to determine from bus activity whether or not a branch is taken or a prefetch is executed. In these cases, the inverse assembler marks the disassembled line with the "?" prefix.

The logic analyzer captures prefetches, even if they are not executed. Care must be taken when you are specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches at most two words, one technique to avoid unwanted triggering from unused prefetches is to add "4" to a trigger address in a branch shadow. This trigger condition is only satisfied if the branch is not taken.

Exceptions (!)

When phase two of the IPIPE signals indicate that an exception has been recognized, the inverse assembler marks the state with a "!" prefix.

Error Messages

The following list of messages will help you identify operation errors.

Data Error — Trace data collected by the logic analyzer cannot be retrieved from memory. Indicates a hardware error or inverse assembler software error.

Illegal Opcode — Undefined opcode encountered. Microprocessor action cannot be determined.

Note 

Do not modify bits 0 - 15 in the ADDR, DATA, or STAT labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Also note that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

3

General Information

Introduction

This chapter contains the characteristics and signal mapping for the HP E2419A Preprocessor Interface.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2419A Preprocessor Interface. These characteristics are included as additional information for the user.

Product Compatibility: Motorola MC68HC16 microprocessors and MC68HC16 EVB.

Microprocessor Package: 132-pin PQFP.
132-pin CQFP.

Accessories Required: None.

Clock Speed: 16 MHz CLK (8 MHz AS rate).

Note 

On a read cycle, data must be valid for 10 ns before the rising edge of AS for all logic analyzers except the HP 1660A/61A/62A, HP 16540/16541A,D, HP 16542A, and HP 16550A.

Signal Line Loading: 100 kΩ plus 8 pF on all lines.

Power Requirements: 1.0 mA at 5 Vdc from the logic analyzer.

Logic Analyzer Required: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D (Master Card and one or two expansion cards), HP 16542A (Master Card and two or three expansion cards), or HP 16550A.

Number of Probes Used: Up to six 16-channel probes. Only three are required for inverse assembly.

Microprocessor Operations Displayed:	Program Read Unused Prefetch Data Read Data Write	
Additional Capabilities:	The logic analyzer captures all bus cycles, including prefetches.	
Environmental Temperature:	Operating:	0 to + 55 °C (+ 32 to + 131 °F)
	Nonoperating:	–40 to + 75 °C (–40 to + 167 °F)
Altitude:	Operating:	4,600 m (15,000 ft)
	Nonoperating:	15,300 m (50,000 ft)
Humidity:	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Clocking

The microprocessor's address strobe (AS) indicates that address, function code, size, and R/W state information are on the bus and valid. The logic analyzer uses the rising edge of AS to clock information into the logic analyzer.

Signal-to-Connector Mapping

Table 3-2 describes the electrical interconnections implemented with the HP E2419A Preprocessor Interface. The signals are listed according to the pod numbers of the preprocessor interface. The pods on the MC68HC16 EVB are numbered differently than the pods on the preprocessor interface. Table 3-1 lists the correlation between the MC68HC16 EVB pod numbers and the preprocessor interface pod numbers.

Since the pods on the logic analyzers may be numbered differently than the pods on the preprocessor interface, refer to table 1-1 or 1-2 to correlate the pod numbers.

Table 3-1. Pod Number Correlation

Microprocessor Signals	Preprocessor Interface Pod Number	MC68HC16 EVB Pod Number
DATA	P1	P2
ICx	P2	P4
ADDR (low)	P3	P1
ADDR (high)	P4	P3
STAT	P5	P5
IRQ	P6	P6

Table 3-2. Signal-to-Connector List

E2419A Pod/ Connector Pin	Logic Analyzer Probe	68HC16 Pin/ E2419A PGA Pin	Pin Mnemonic	Label
P1 / 19	0	109 / J1	D0	DATA
P1 / 18	1	108 / H3	D1	DATA
P1 / 17	2	107 / H4	D2	DATA
P1 / 16	3	106 / H1	D3	DATA
P1 / 15	4	104 / G3	D4	DATA
P1 / 14	5	103 / G4	D5	DATA
P1 / 13	6	102 / G1	D6	DATA
P1 / 12	7	101 / G2	D7	DATA
P1 / 11	8	100 / G5	D8	DATA
P1 / 10	9	99 / F2	D9	DATA
P1 / 9	10	96 / F3	D10	DATA
P1 / 8	11	95 / E2	D11	DATA
P1 / 7	12	94 / E1	D12	DATA
P1 / 6	13	93 / E4	D13	DATA
P1 / 5	14	92 / E3	D14	DATA
P1 / 4	15	91 / D2	D15	DATA
P2 / 19	0	7 / M8	IC1	(Note 1)
P2 / 18	1	6 / L8	IC2	(Note 1)
P2 / 17	2	5 / K7	IC3	(Note 1)
P2 / 16	3	4 / J7	OC1	(Note 1)
P2 / 15	4	3 / M7	OC2	(Note 1)
P2 / 14	5	132 / L6	OC3	(Note 1)
P2 / 13	6	131 / M6	OC4	(Note 1)
P2 / 12	7	130 / J6	IC4 / OC5	(Note 1)

Note 1: These signals are not required for inverse assembly. However, they may be useful for microprocessor analysis.

Table 3-2. Signal-to-Connector List (Continued)

E2419A Pod/ Connector Pin	Logic Analyzer Probe	68HC16 Pin/ E2419A PGA Pin	Pin Mnemonic	Label
P2 / 11	8	129 / K6	PAI	(Note 1)
P2 / 10	9	128 / L5	PWMA	(Note 1)
P2 / 9	10	127 / M5	PWMB	(Note 1)
P2 / 8	11	126 / J5	PCLK	(Note 1)
P2 / 7	12	17 / M12	RXD	(Note 1)
P2 / 6	13	69 / A6	RESET	(Note 1)
P2 / 5	14	65 / A7	TSTME / TSC	(Note 1)
P2 / 4	15		(no connection)	
P3 / 19	0	90 / D1	A0	ADDR
P3 / 18	1	19 / K11	A1	ADDR
P3 / 17	2	20 / K10	A2	ADDR
P3 / 16	3	23 / J9	A3	ADDR
P3 / 15	4	24 / J12	A4	ADDR
P3 / 14	5	25 / J11	A5	ADDR
P3 / 13	6	26 / H10	A6	ADDR
P3 / 12	7	27 / H9	A7	ADDR
P3 / 11	8	28 / H12	A8	ADDR
P3 / 10	9	30 / G10	A9	ADDR
P3 / 9	10	31 / G9	A10	ADDR
P3 / 8	11	32 / G12	A11	ADDR
P3 / 7	12	33 / G11	A12	ADDR
P3 / 6	13	34 / F8	A13	ADDR
P3 / 5	14	35 / F11	A14	ADDR
P3 / 4	15	36 / F12	A15	ADDR

Note 1: These signals are not required for inverse assembly. However, they may be useful for microprocessor analysis.

Table 3-2. Signal-to-Connector List (Continued)

E2419A Pod/ Connector Pin	Logic Analyzer Probe	68HC16 Pin/ E2419A PGA Pin	Pin Mnemonic	Label
P4 / 19	0	37 / F9	A16	ADDR (Note 1)
P4 / 18	1	38 / F10	A17	ADDR (Note 1)
P4 / 17	2	39 / E11	A18	ADDR (Note 1)
P4 / 16	3	119 / K3	A19 / CS6	ADDR (Note 1)
P4 / 15	4	120 / M3	A20 / CS7	ADDR (Note 1)
P4 / 14	5	121 / K4	A21 / CS8	ADDR (Note 1)
P4 / 13	6	122 / J4	A22 / CS9	ADDR (Note 1)
P4 / 12	7	123 / M4	A23 / CS10	ADDR (Note 1)
P4 / 11	8	63 / C7	CLKOUT	(Note 1)
P4 / 10	9	110 / J3	CSBOOT	(Note 1)
P4 / 9	10	117 / M2	BG / CS1	(Note 1)
P4 / 8	11	116 / M1	BR / CS0	(Note 1)
P4 / 7	12	86 / C3	DS	(Note 1)
P4 / 6	13	85 / C2	AS	(Note 1)
P4 / 5	14	70 / D6	HALT	(Note 1)
P4 / 4	15	87 / C1	AVEC	(Note 1)
P5 / 19	0	118 / L3	BGACK / CS2	STAT
P5 / 18	1	80 / A3	R/W	STAT
P5 / 17	2	82 / A2	SIZ0	STAT
P5 / 16	3	81 / B2	SIZ1	STAT
P5 / 15	4	111 / J2	FC0 / CS3	STAT
P5 / 14	5	114 / L2	FC1 / CS4	STAT
P5 / 13	6	115 / L1	FC2 / CS5	STAT
P5 / 12	7	89 / D4	DSACK0	STAT

Note 1: These signals are not required for inverse assembly. However, they may be useful for microprocessor analysis.

Table 3-2. Signal-to-Connector List (Continued)

E2419A Pod/ Connector Pin	Logic Analyzer Probe	68HC16 Pin/ E2419A PGA Pin	Pin Mnemonic	Label
P5 / 11	8	88 / D3	DSACK1	STAT
P5 / 10	9	68 / B6	IPIPE1/DSI	STAT
P5 / 9	10	67 / E6	IPIPE0/DSO	STAT
P5 / 8	11	*	IPIPE1 LATCH	STAT
P5 / 7	12	*	IPIPE0 LATCH	STAT
P5 / 6	13	64 / D7	FREEZE/QUOT	STAT
P5 / 5	14	66 / B7	BKPT/DSCLK	STAT
P5 / 4	15	71 / C6	BERR	STAT
P6 / 19	0	11 / K9	MOSI	(Note 1)
P6 / 18	1	10 / M9	MISO	(Note 1)
P6 / 17	2	12 / L9	SCK	(Note 1)
P6 / 16	3	16 / M11	PCS3	(Note 1)
P6 / 15	4	15 / L11	PCS2	(Note 1)
P6 / 14	5	14 / M10	PCS1	(Note 1)
P6 / 13	6	13 / L10	PCS0/SS	(Note 1)
P6 / 12	7	18 / L12	TXD	(Note 1)
P6 / 11	8	72 / B5	IRQ7	(Note 1)
P6 / 10	9	73 / A5	IRQ6	(Note 1)
P6 / 9	10	74 / D5	IRQ5	(Note 1)
P6 / 8	11	75 / C5	IRQ4	(Note 1)
P6 / 7	12	76 / A4	IRQ3	(Note 1)
P6 / 6	13	77 / C4	IRQ2	(Note 1)
P6 / 5	14	78 / B4	IRQ1	(Note 1)
P6 / 4	15	79 / B3	MODCLK	(Note 1)

* Latched version of IPIPE0/1.
Note 1: These signals are not required for inverse assembly. However, they may be useful for microprocessor analysis.

Table 3-2. Signal-to-Connector List (Continued)

E2419A Pod/ Connector Pin	Logic Analyzer Probe	68HC16 Pin/ E2419A PGA Pin	Pin Mnemonic	Label
P1 / 3	CLK	85 / C2	AS	
P3 / 3	CLK	88 / D3	DSACK1	
P4 / 3	CLK	89 / D4	DSACK0	
P5 / 3	CLK	63 / C7	CLKOUT	
P6 / 3	CLK	86 / C3	DS	

Servicing

The repair strategy for the HP E2419A is board replacement. However, table 3-3 lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Table 3-3. Replaceable Parts

HP Part Number	Description
E2413-66504	Logic Analyzer Interface Board
E2419-66503	MC68HC16 Interface Board
E2419-68702	Inverse Assembler Disk Pouch
E3417A	132-pin QFP Probe Adapter Assembly
1200-1657	Pin Protector IC Socket

Dimensions

Figure 3-1 lists the dimensions for the HP E2419A circuit board. The dimensions are listed in inches and millimeters.

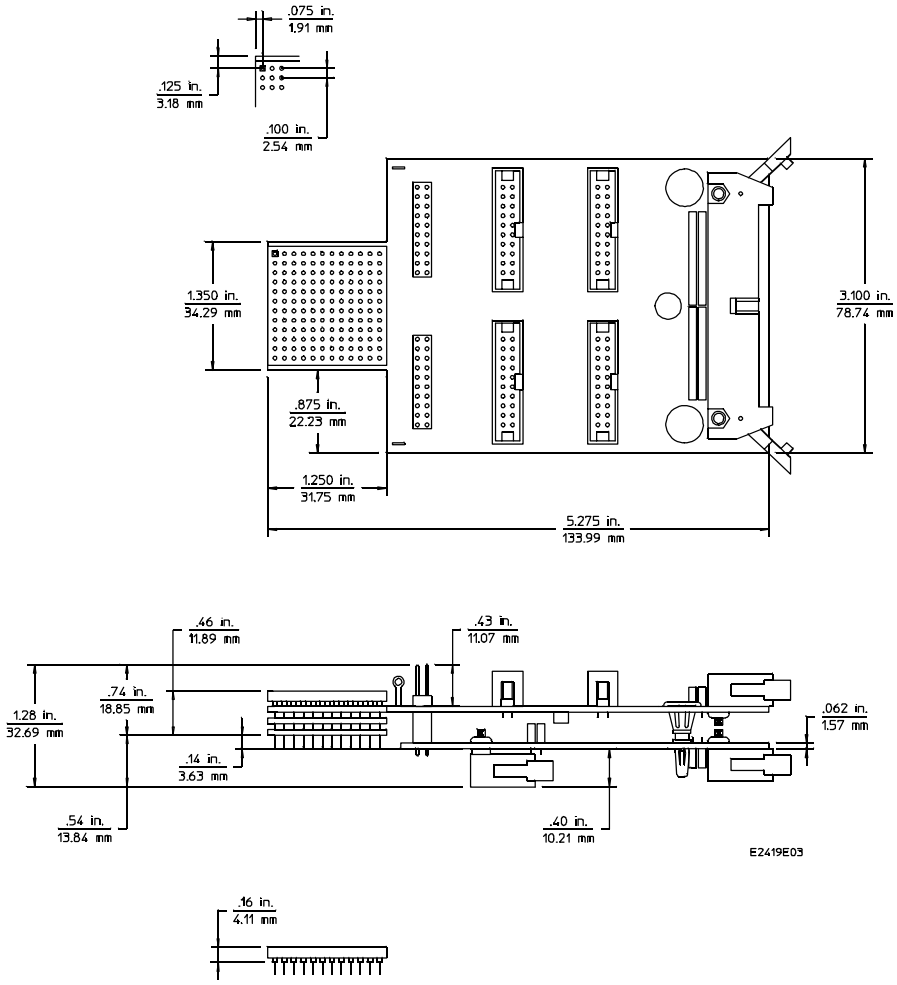

Figure 3-1. HP E2419A Dimensions

A

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").

"Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500/16501 frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly. Ensure that the target system is on and operating properly.

If the error message persists, check the that the logic analyzer pods are connected to the proper connectors, as listed in table 1-1 or 1-2.

For HP 1650A and HP 16510A Logic Analyzers, check the preprocessor interface power fuse in the logic analyzer.

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500 disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the input cursor) and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that all microprocessor caches and memory managers have been disabled. In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading. The following techniques will reduce the capacitive loading:

- Remove as many pin protectors, extenders, and adapters as possible.
- If multiple preprocessor interface solutions are available, try using one with lower capacitive loading.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

Note 

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to < 60 ns. If this error message is observed with the Clock Period set to > 60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message indicates:

- For an HP 16511B Logic Analyzer, only one of the two cards is receiving its state clock. Refer to "Slow or Missing Clock."
- For an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer, the pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen

The HP 16540/16541A,D or HP 16542A Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded" (16540/41/42)

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16540A,D, HP 16541A,D or HP 16542A cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.